Short Papers

Monolithic 2–18 GHz Matrix Amplifiers

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Abstract—**The designs and performances of two different monolithic 2–18 GHz matrix amplifiers are discussed. The first module, optimized for gain and return loss, yields gains of $G = 15.5 \pm 0.9$ dB and a maximum return loss of $RL = -12.0$ dB. When cascading these modules to form a two- or three-stage amplifier, gains of $G = 31.4 \pm 1.4$ dB and $G = 43.2 \pm 1.8$ dB are measured. With the second unit, designed for low noise and gain, noise figures of $NF = 4.15 \pm 0.85$ dB and gains of $G = 17.1 \pm 1.25$ dB were achieved.**

I. Introduction

The principle of the matrix amplifier and its performance when using hybrid circuit technology have been widely discussed in the literature [1]–[3]. High gains and low noise figures have been achieved with two- and three-tier hybrid circuits across multioctave frequency bands, making this new type of amplifier a powerful competitor whenever these qualities are of major concern [3] and [4].

Very recently, the first monolithic matrix amplifiers have emerged [5], [6]. This paper discusses the design and the experimental results of two monolithic 2×4 amplifier modules. The first module was strictly designed for gain and *VSWR* performance, while in the case of the second unit the major emphasis was shifted to the optimization of the noise figure. Both amplifier modules employ MESFET's with 0.35×200 μm^2 gates as active devices; however, they have different topologies.

II. Circuit Design and Fabrication

The concept of the matrix amplifier integrates the principles of additive and multiplicative amplification in one and the same module [1], [2]. The resulting circuit forms a network in which the active devices are positioned in a rectangular array. A schematic of the 2×4 matrix amplifiers to be discussed in this paper is shown in Fig. 1. A photograph of the 1.9×2.3 mm^2 chip of the first module, designed for optimum gain and return loss, and of the 2.2×2.4 mm^2 chip of the low-noise module is presented in Fig. 2. It reflects the layouts and the line dimensions of these circuits. A total of four identical MESFET's are located in each of two tiers and are linked horizontally as well as vertically by transmission line elements. Each idle port is terminated into either a resistor or an impedance consisting of a resistor shunted by a shorted transmission line. This technique allows biasing of the active devices without any power dissipation in the termination resistors. The choice for the termination elements is critical for gain flatness, noise figure, and gain slope, as well as for stability. The sources of all MESFET's are coupled to ground through thin-film capacitors and via holes. They are clearly visible in the photograph of Fig. 3, which shows the monolithic chips brazed to alumina substrates. The latter contain part of the

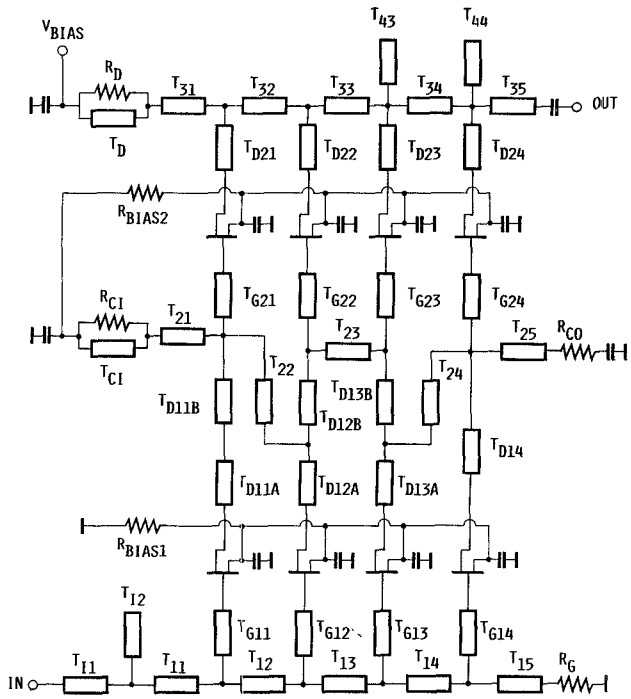

Fig. 1. Schematic of the matrix amplifiers, including the biasing scheme.

biasing circuitry, including the source bias resistors, as well as the input and output lines. Separating the biasing network from the monolithic chip and fabricating it on the alumina substrate serves two purposes. First, it provides for an option to moderately tune the circuit and, therewith, improve the amplifier's gain flatness and reflection losses. Second, it significantly reduces the overall chip size and, consequently, the chip costs. The first function may become a decisive factor in the success or the failure of meeting the required performance specifications, which, of course, depend heavily on the uniformity and repeatability of the active devices' parameters. The amplifiers are energized by a single dc voltage in accordance with the schematic of Fig. 1 such that the same dc current passes through both tiers.

The processing for these circuits is performed on undoped LEC GaAs wafers with an MBE-grown active layer doped at 4.4×10^{17} cm^{-3}. Device isolation is achieved with oxygen implantation followed by a low-temperature anneal. Ohmic contacts to the active layer are formed using a standard NiAuGe alloy technique, and precision thin-film resistors are patterned from a reactively sputtered TiWN barrier film which is chemically stable against a GaAs surface. The 0.35 μm aluminum Schottky gates are patterned using a photolithographic technique involving ammonia image reversal and a controlled erosion step to define a 0.35 μm feature that is transferred to the wafer surface [7]. The devices are passivated with plasma CVD silicon nitride, which serves to encapsulate the FET devices and provides a thin-film capacitor dielectric. After two additional levels of interconnect metallization are processed, the wafer is given a protection coating and reverse mounted for back-side processing. The wafer is then lapped to 4.5 mils, and laser drilled to provide 60-μm-diameter contact holes to the front-side ground pads. This is followed

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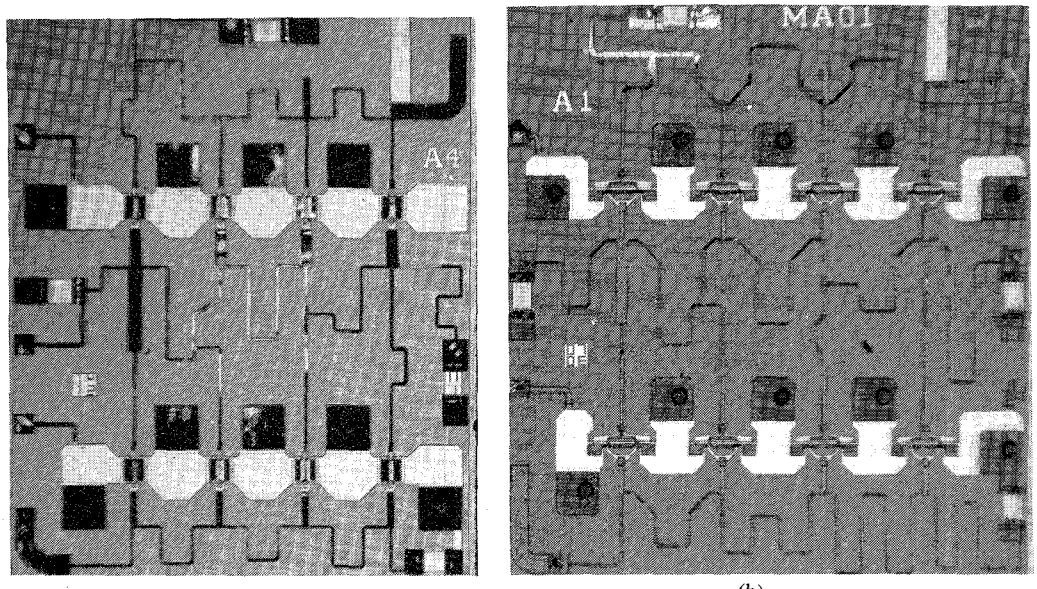

(a) (b)

Fig. 2. Photograph of (a) the monolithic high-gain/low-*VSWR* chip and (b) the low-noise/high-gain chip.

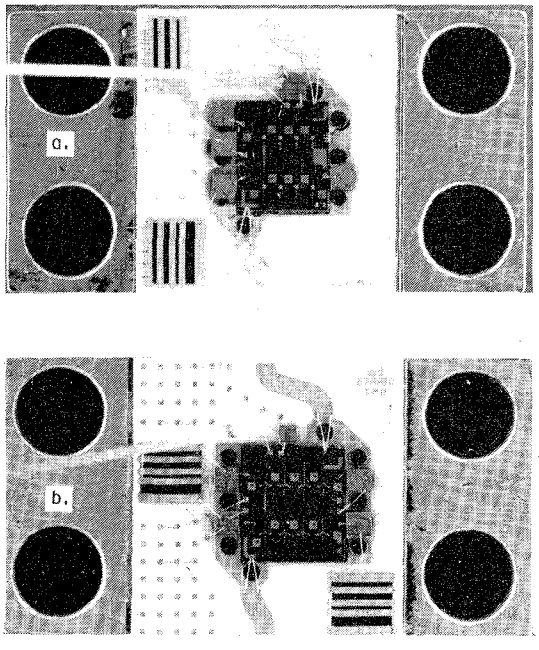

Fig. 3. Photograph of (a) the high-gain/low-*VSWR* module and (b) the low-noise/high-gain module.

by a back-side plating step, demount, and saw for die separation. The 0.35×200 μm^2 FET devices exhibit a $g_m = 42$ mS, $C_{gs} = 170$ fF, $C_{gd} = 14$ fF, $C_{ds} = 35$ fF, and $R_{ds} = 280$ Ω as determined from on-wafer RF probing.

The computed gain characteristics of the amplifier modules are shown in Fig. 4 and Fig. 8. Based on these computations a gain of $G = 16.2 \pm 0.9$ dB across the 2–18 GHz frequency band for the unit optimized for gain was expected. Similarly, according to the computed performance characteristics of the module that was optimized for low-noise performance, gains of $G = 15.9 \pm 0.9$ dB

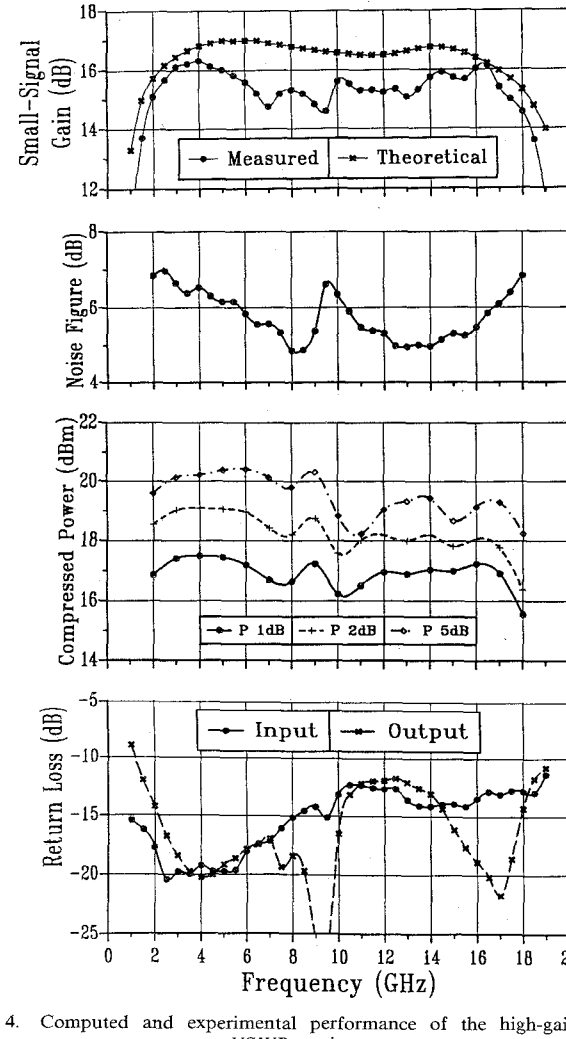

Fig. 4. Computed and experimental performance of the high-gain/low-*VSWR* version.

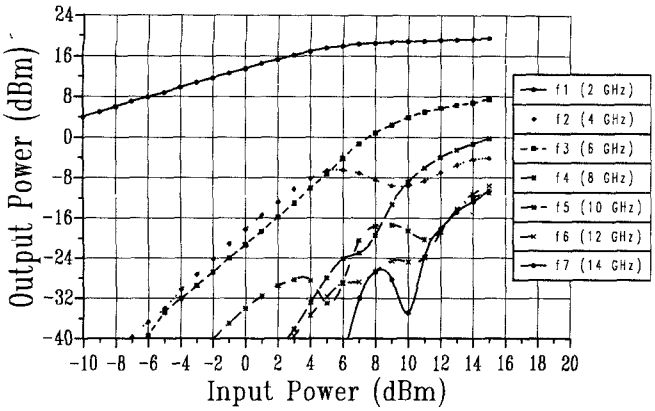

Fig. 5. Measured harmonic output powers as a function of input power ($f = 2$ GHz).

and a maximum noise figure of $NF = 5.4$ dB were predicted across the same band. MESFET's with the gate dimensions of $0.35 \times 200\ \mu m^2$ were used in both amplifier modules; however, as shown in the photograph of Fig. 2, the U-shaped gate of the first circuit was replaced by the π-shaped gate topology of the low-noise version, resulting in a lower-gate resistance. All amplifier units were biased by a single voltage in accordance with the schematic of Fig. 1.

III. Experimental Results

A. Design for Optimized Gain and VSWR Performance

The test results of the first experimental monolithic matrix amplifier, as it is shown in Fig. 3(a), are plotted in Fig. 4. The unit's supply voltage and current in our tests were $V_{BIAS} = 9.0$ V and $I_{BIAS} = 108$ mA, respectively. A small-signal gain of 15.5 ± 0.9 dB and a maximum noise figure of 7 dB were recorded over the 2–18 GHz bandwidth. The maximum return loss was -12.5 dB for the input and -12.0 dB for the output port, corresponding to *VSWR*'s of 1.62:1 and 1.67:1, respectively. The output powers at the 1 dB, 2 dB, and 5 dB compression points are also plotted in the curves of Fig. 4 which show minimum levels at 15.5 dBm, 16.5 dBm, and 18.2 dBm, respectively. As demonstrated in Fig. 5, at compression levels of up to 5 dB and at an input signal frequency of $f = 2$ GHz, the worst-case harmonic's output power does not exceed -15 dBc. We have found this relatively low harmonic content to be a characteristic of all matrix amplifiers tested to date. The measured third-order intercept points of this unit are at a minimum of 32 dBm for fundamental input signal frequencies between $f = 2$ GHz and $f = 7$ GHz. As demonstrated in the plots of Fig. 6, the small-signal gain and the noise figure vary fairly uniformly while the 1 dB compressed output power changes very little over the temperature range of -55°C to $+95$°C. An attempt to cascade two and three of the modules shown in Fig. 3(a) resulted in the measured data plotted in Fig. 7. As demonstrated, the two-stage amplifier exhibits an overall gain of $G = 31.4 \pm 1.4$ dB while that of the three-stage unit is $G = 43.2 \pm 1.8$ dB. The respective worst-case return losses were measured at the input ports, namely, $RLI = -11.1$ dB and $RLI = -12.0$ dB.

B. Design for Optimized Noise Figure and Gain Performance

The measure data of the second monolithic 2–18 GHz matrix amplifier, designed with major emphasis on its low-noise performance are summarized in the plots of Fig. 8. Measurements of

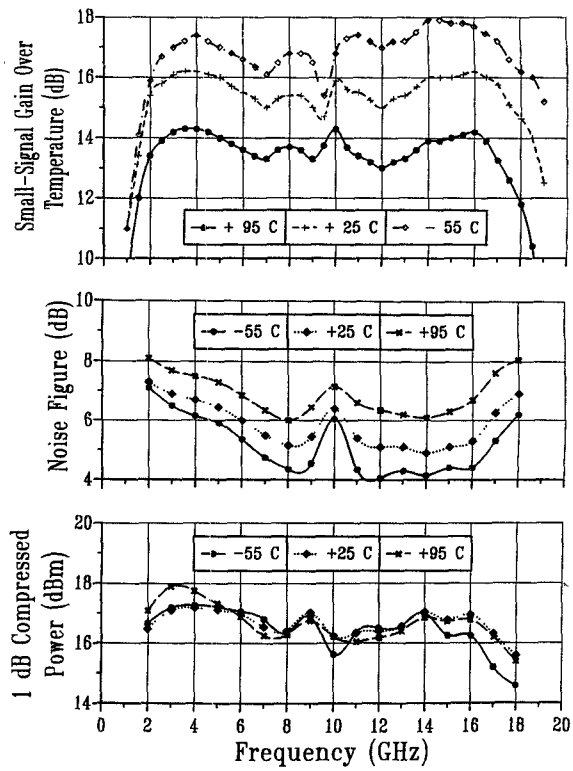

Fig. 6. Measured gain, noise figure, and output power as a function of temperature.

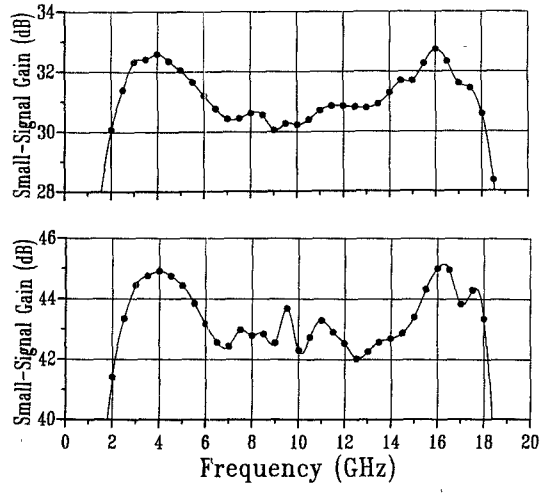

Fig. 7. Experimental gain of the two-stage amplifier and the three-stage amplifier.

this module show significant improvements in noise figure when compared to the unit described earlier. At gains of $G = 17.1 \pm 1.25$ dB and a maximum return loss of $RL = -10.2$ dB, noise figures of $NF = 4.15 \pm 0.85$ dB were achieved across the 2–18 GHz frequency band. A comparison with the data obtained from the first design in Fig. 4 shows a 2.0 dB improvement of the maximum noise figure and a 1.25 dB increase in the minimum gain. However, the maximum input and output return losses have deteriorated by 2.3 dB and 1.8 dB, respectively, while the gain variation has increased from ± 0.9 dB to ± 1.25 dB.

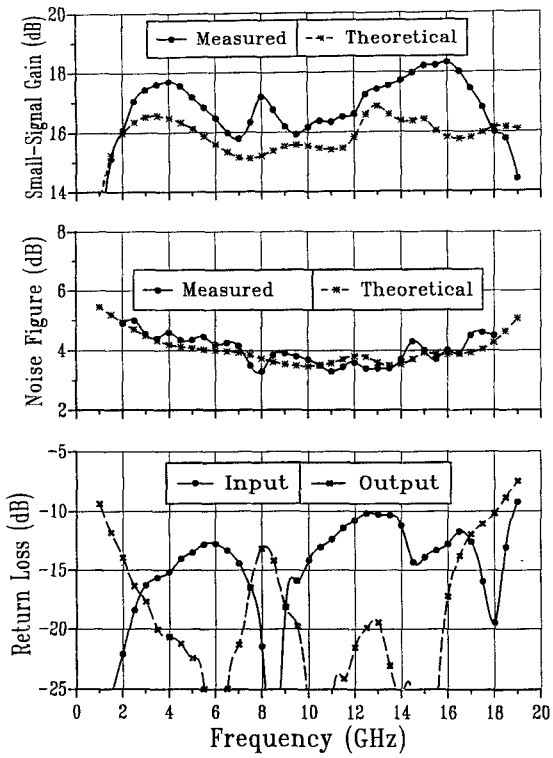

Fig. 8 Computed and experimental performance of the low-noise/high-gain module.

IV. Conclusion

An effort to develop monolithic 2–18 GHz matrix amplifiers has resulted in the successful fabrication of a high-gain/low-*VSWR* and a high-gain/low-noise module across the 2–18 GHz frequency band. The experimental results achieved represent the highest gains and lowest noise figures reported to date in monolithic 2–18 GHz amplifier modules using MESFET's.

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Monolithic GaAs p-i-n Diode Switch Circuits for High-Power Millimeter-Wave Applications

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***Abstract*—Two different *Ka*-band SPDT switch circuits using monolithic GaAs epitaxial p-i-n diode technology are presented. The lowest insertion loss is 0.7 dB at 35 GHz, and isolation is better than 32 dB from 30 to 40 GHz. The power handling capability is at least +38 dBm pulsed and +35 dBm CW. Switching speed rise and fall times are 2 ns.**

I. Introduction

The degree to which a millimeter-wave radar system can accurately locate a moving object is, in large part, dependent upon the RF transceiver section of the system. The transceiver performs the important function of interfacing computer processing and control with the transmitted and reflected radar signals. One of the more fundamental functions of a transceiver is to route signals from the antenna to the transmitter or receiver. The RF switch employed for this purpose should have low insertion loss and high power handling capabilities. A low-loss, high-power switch in the RF transceiver section is essential in realizing the full potential of a millimeter-wave system.

In this paper we describe the development and testing of monolithic SPDT switches designed to meet the progressively increasing power requirements of developing millimeter-wave systems. Previous work has been reported on monolithic switch circuits employing planar p-i-n structures [1], [2] or MESFET devices [3]. The switches presented here employ epitaxial vertical p-i-n diode structures [4] in a shunt configuration optimized for low loss and high isolation under high-power signal conditions. The vertical epitaxial structure is expected to provide lower RF impedance under forward bias than planar ion-implanted p-i-n structures [5] and to have power handling capability superior to that of MESFET's. An additional feature of the circuits described here is the location of the p-i-n diode directly underneath the RF line. This can improve isolation and increase bandwidth compared to planar devices, which are typically positioned adjacent to, or a quarter-wave from, the RF line.

II. Circuit Description

Fig. 1 illustrates the two SPDT designs investigated in this work. Each output arm contains a p-i-n diode spaced a quarter-wavelength from the common input arm. When forward biased, the low-impedance p-i-n diode is transformed through the quarter-wave section to present a high impedance at the switch junction. Simultaneously, the junction capacitance of the reverse-biased p-i-n in the second arm is tuned to a low-pass filter response by the inductive air bridge interconnects. In Fig. 1(a) via holes are used to ground the diodes while the design in Fig. 1(b) uses radial stubs to provide the RF ground at the diodes.

Insertion losses associated with the prototype design can be optimized by properly selecting the elements for a low ripple Chebyshev response. Analysis by computer predicts that most of the critical dimensions in the circuit depend upon the diode parameters. In order to reduce the amount of empirical work

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